DIGITAL HIGH SPEED PROGRAMMABLE DELAYED LOCKED LOOP

ABSTRACT OF THE DISCLOSURE

A digital high speed programmable delayed locked loop (DLL) includes a zero degree phase shift digital delay line, at least one intermediate phase shift digital delay line, a three hundred and sixty degree phase shift digital delay line, and a digital control module. The zero degree phase shift, intermediate phase shift, and 360 degree phase shift digital delay lines are operably coupled to produce, from a clock signal, zero phase shifted, intermediate phase shifted, and 360 phase shifted representations, respectively, of the clock signal. The digital control module is operably coupled to produce an intermediate control signal for the intermediate phase shift digital delay line and a 360 degree control signal for the 360 degree phase shift digital delay line based on a phase difference between the zero phase shifted representation of the clock signal and the three hundred and sixty degree phase shifted representation of the clock signal.